VC0706

Digital Video Processor

Datasheet

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1. GENERAL DESCRIPTION

VC0706 is a high performance camera processor with enhanced image processing functions. This SOC chip has CMOS sensor interface and digital video input interface, can capture the video stream from CMOS sensor or external TV decoder, implement video enhancement, OSD overlay and motion detection, before output the digital video through the CCIR656 output interface, make VC0706 can easily to be connected to external DSP/host processor for further video processing, such as the compression and broadcast. External host processors can control the VC0706 through the flexible SPI/UART interface.

VC0706 embedded the hard-wired JPEG codec, supports up to 30fps encoding or decoding with the VGA resolution. VC0706 can compress the captured video stream to M-JPEG stream and output through the SPI/UART interface, or receive M-JPEG stream written by external host, before decoding and output.

VC0706 embedded TV encoder and video DAC, make it can output NTSC/PAL video to TV monitors or other 75ohm display devices directly.

VC0706 can be easily to be applied in security camera, automotive camera or and embedded camera require image pre-processing & M-JPEG compression.

Below are VC0706's key parameters:

PARAMETERS	VALUES	UNIT
Sensor Type Supported	VGA/CIF CMOS	
NTSC (M) output	712 x 486	Pixel
PAL (B) output	704 x 576	Pixel
Maximum Frame Rate	60 (@ 27MHz in NTSC) 50 (@ 27MHz in PAL)	fps
Maximum SPI Interface Clock Frequency	18	Mhz
Maximum HS-UART Interface BPS	921.6	kbps
Power consumption	65	mA
Crystal input Frequency	6.0	MHz
Power Supply	3.3 & 1.2	V
Operating Temperature	-40 ~ +85	℃

VC0706 has two variations listed in the table below:

PRODUCT NUMBER	PACKAGE
VC0706PREA	100-Pin LQFP (14mm x 14mm x 1.4mm)
VC0706PTNA	144-Pin LQFP (20mm x 20mm x 1.4mm)

2. FULL FEATURE LIST

- Video Input
  - ✧ Support up to VGA CMOS sensor
  - ✧ Support CCIR656 input from external TV decoder
- Video Out
  - ✧ Digital video output
    - ■ CCIR656 digital video output interface
  - ✧ Analog video output
    - ■ BT.470 compatible analog composite video output: NTSC or PAL
    - ■ Support 8-bit key protect video encryption output mode
    - ■ Support NTSC-M/J/4.43 and PAL-/B/D/G/H/M/N/I/Nc TV video
  - ✧ Compressed video output
    - ■ JPEG format
    - ■ Resolution and compression ratio configurable
- Video steam frame rate control
- Image process pipeline
  - ✧ Black level correction with G1/G2 filter
  - ✧ Auto Exposure (AE)
  - ✧ Auto White Balance (AWB)
  - ✧ Auto Gain Control (AGC)
  - ✧ Auto defect pixel detection and cancellation
  - ✧ Auto lens shading compensation
  - ✧ Auto edge extraction and sharpness processing
  - ✧ Auto false color suppression
  - ✧ Auto backlight detection and wide dynamic range compensation
  - ✧ Advanced noise reduction for high image quality under low light
  - ✧ Auto UV suppression under low light
  - ✧ Configurable gamma and color correction
  - ✧ Configurable brightness, contrast, hue, saturation control
  - ✧ Edge-adaptive CFA interpolation
  - ✧ Up to 16-window for statistical collection, exposure
  - ✧ Color/BW video image auto/manual conversion
- Motion detection
  - ✧ 4x4 window, sensitivity programmable
  - ✧ Support both horizontal and vertical calculation
  - ✧ The window size, location can be programmable
  - ✧ The motion detection function can be enabled and disable by window
  - ✧ The threshold of each motion detection window can be set separately
  - ✧ Slight illumination changes alarm cancellation when no motion
  - ✧ Support separate motion detection threshold to adjust post process frame rate

- Flexible image scalar
  - ✧ Support 1:1, 2:1, 4:1 horizontally and vertically down-scalar of input image
  - ✧ Support scale for D1 resolution output
    - ■ Arbitrary ratio scale-up
    - ■ Maximum 2 times scale-down
- On Screen Display
  - ✧ Up to four OSD channels supported with separate control
    - ■ One character channel support up to 4 lines
    - ■ One static graphic channel for the usage of user programmable logo
    - ■ One mosaic channel for the usage of private area protection
    - ■ One bitmap channel support real time display the bitmap
  - ✧ Rich control features for each channel
  - ✧ Built-in character library with totally 80 characters
- Build-in 8-bit MCU
  - ✧ High performance MCU core with rich peripherals
  - ✧ On-chip SRAM & program code ROM
  - ✧ Support disable mask ROM and run program code from external flash
    - ■ Separate code memory and data memory chip select signal
    - ■ Separate address bus and data bus
    - ■ Support the encryption of external ROM code to protect customers intellectual property
    - ■ Address space extension via page mode
- High speed SPI Interface
  - ✧ Master/Slave mode selectable
  - ✧ Programmable bit clock supported up to 18MHz
  - ✧ Support both host and DMA work mode
  - ✧ DMA channel between OSD bitmap channel and SPI
  - ✧ Bi-direction DMA channel between FBUF and SPI
- High speed UART Interface
  - ✧ Programmable bit rate supported up to 921.6 kbps
  - ✧ Bi-direction DMA channel between FBUF and UART
- Flexible GPIO function configuration mechanism support rich features
  - ✧ Backlight compensation enable
  - ✧ Mirror control
  - ✧ AE indoor/outdoor switch
  - ✧ Motion enable
  - ✧ Motion output
  - ✧ Color or Black & White output selection
- One input clock: 6MHz crystal
- Configurable I2C EEPROM, SPI EEPROM/FLASH

3. CHIP BLOCK DIAGRAM

VC0706 integrates SIF (sensor interface), ISP (image signal processor), frame rate control unit, Video Enhancement Engine, JPEG codec, Motion Detection Engine, IPP (image post-processor), OSD unit, TV encoder, Video DAC and 8051 compatible MCU with built-in code-ROM and data-RAM.

The CCIR656 output interface enable VC0706 output enhanced digital video stream to external DSP or host CPU for compression or broadcast.

The bi-direction DMA path between FBUF and SPI/HS-UART enable the external processor read out the captured JPEG image or write JPEG pictures for display.

With the DMA channel between SPI interface and OSD unit, VC0706 can be easily used to implement static or dynamic bitmap overlay with real time video data from sensor.

The behaviors of VC0706 can be programmed through I2C EEPROM, SPI EEPROM/FLASH , and external host processor . Multiple GPIO channels support typical control functions.

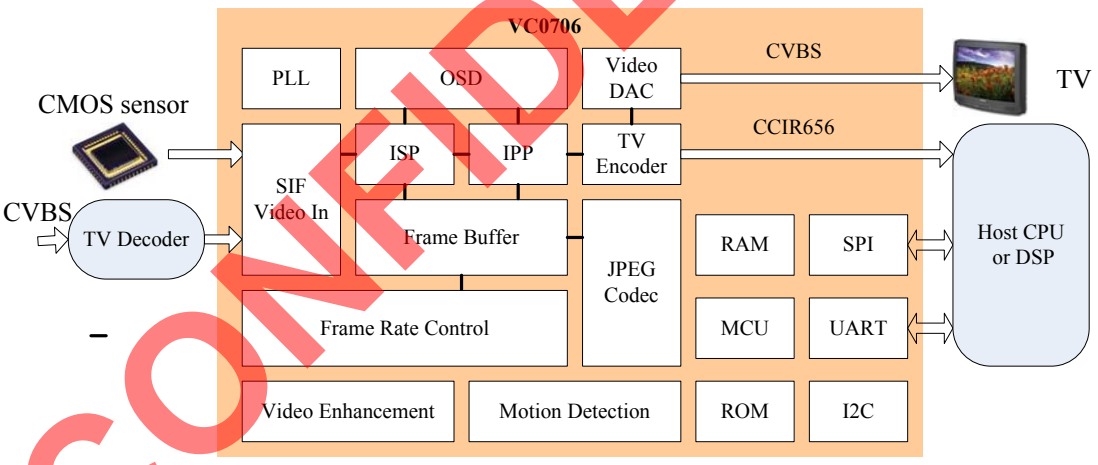


Figure 1: VC0706 Chip Block Diagram

4. PIN ASSIGNMENTS

4.1 VC0706PREA Pin Assignments

PIN NUMBER VC0706PRSA	NAME	TYPE	DESCRIPTION
1	CS_SDA	I/O, OD , S	Sensor I2C bus SDA pin
2	GPIO13	I/O, PD	GPIO 13
3	CS_SCK	I/O, OD , S	Sensor I2C bus SCK pin
4	GPIO12	I/O , PD	GPIO 12
5	CS_HSYNC	I, PD	Sensor Horizontal sync input
6	MCU_WEN	O	MCU NOR flash interface write enable signal "0" indicate write operation; "1" indicate read operation
7	CS_VSYNC	I, PD	Sensor vertical sync input
8	MCU_A15	O	MCU NOR flash interface address bit 15
9	MCU_A14	O	MCU NOR flash interface address bit 14
10	CS_PCLK	I, PD	Sensor pixel clock input
11	CS_CLK	O	Sensor CLK output
12	GPIO9	I/O , PD	GPIO 9
	OSD_RDY	O	Ready to accept new OSD data from host through SPI interface
13	CS_D0	I, PD	Sensor data input bit 0
	CS_PCLK	I, PD	Sensor pixel clock input
14	MCU_DCEN	O	MCU NOR flash interface data memory chip select , "0" valid
15	CS_D1	I, PD	Sensor data input bit 1
16	CS_D2	I, PD	Sensor data input bit 2
17	MCU_A13	O	MCU NOR flash interface address bit 13
18	MCU_A12	O	MCU NOR flash interface address bit 12
19	CS_D3	I, PD	Sensor data input bit 3
20	CS_D4	I, PD	Sensor data input bit 4
21	MCU_A11	O	MCU NOR flash interface address bit 11
22	MCU_A10	O	MCU NOR flash interface address bit 10
23	CS_D5	I, PD	Sensor data input bit 5

PIN NUMBER			
24	CS_D6	I, PD	Sensor data input bit 6
25	MCU_A9	O	MCU NOR flash interface address bit 9
26	GPIO8	I/O, PD	GPIO 8
	OSD_STOP	I, PD	Host asserted signal to stop OSD DMA
27	MCU_A8	O	MCU NOR flash interface address bit 8
28	CS_D7	I, PD	Sensor data input bit 7
29	CS_D8	I, PD	Sensor data input bit 8
30	CS_D9	I, PD	Sensor data input bit 9
31	MCU_A7	O	MCU NOR flash interface address bit 7
32	MCU_A6	O	MCU NOR flash interface address bit 6
33	CS_PWD	O	CMOS Sensor Power Down Control
	GPIO5	O	GPIO 5 , only can be used as output mode
	TV_HSYNC_O	O	TV encoder HSYNC output
34	CS_RSTB	O	Sensor Reset Output
	TV_MOD	I, PD	Hardware strap pin : TV_MOD
35	MCU_A5	O	MCU NOR flash interface address bit 5
36	MCU_A4	O	MCU NOR flash interface address bit 4
37	GPIO7	I/O , PD	GPIO 7
38	RSTN	I , PU	Power on reset
39	GPIO4	I/O, PD	GPIO 4
	TV_VSYNC_O	O	TV Vertical SYNC Output
	TV_CSYNC_O	O	TV Composite SYNC Output
40	GPIO11	I/O , PD	GPIO 11
41	MCU_A3	O	MCU NOR flash interface address bit 3
42	MCU_A2	O	MCU NOR flash interface address bit 2
43	MCU_A1	O	MCU NOR flash interface address bit 1
	OCODE_MOD	I , PD	Hardware strap pin : OCODE_MOD
44	MCU_A0	O	MCU NOR flash interface address bit 0
	OROM_MOD	I , PD	Hardware strap pin : OROM_MOD
45	VDD_IO	P	Digital IO Power 3.3V
46	VSS	P	Digital IO/core ground
47	VDD	P	Digital core power supply 1.2V
48	VSSA	P	Analog ground

PIN NUMBER			
49	MONA	A	Test signal , not connect
50	VDDA	P	Analog power supply (3.3v)
51	VLX	A	Test signal , not connect
52	VSSA	P	Analog ground
53	DAC_REXT	A	DAC external resistor pin
54	DAC_COMP	A	DAC Compensation pin
55	DAC_CVBS	A, O	CVBS channel signal analog output
56	VSSA_DAC	P	DAC analog ground
57	VDDA_DAC	P	DAC analog Power (3.3V)
58	VSSA_PLL	P	PLL Analog ground
59	VDDA_PLL	P	PLL Analog power (3.3V)
60	TV_D7	O	CCIR656 digital video output bit 7
61	TV_D6	O	CCIR656 digital video output bit 6
62	TV_D5	O	CCIR656 digital video output bit 5
63	TV_D4	O	CCIR656 digital video output bit 4
64	GPIO6	I/O , PD	GPIO 6
	TV_ODD_O	O	TV encoder ODD signal output , “Low” indicate even field , “High” indicate odd field
65	TV_D3	O	CCIR656 digital video output bit 3
66	TV_D2	O	CCIR656 digital video output bit 2
67	GPIO5	O	GPIO 5 , only can be used as output mode
	TV_HSYNC_O	O	TV encoder HSYNC output
	BOOT_MOD	I, PD	Hardware strap pin : BOOT_MOD
68	TV_D1	O	CCIR656 digital video output bit 1
69	TV_D0	O	CCIR656 digital video output bit 0
70	CLK_IN	I	Crystal input
71	CLK_OUT	O	Crystal output (loopback)
72	VSS	P	Digital IO/CORE ground
73	VDD_IO	P	Digital IO Power (3.3v)
74	TV_PCLK	O	Digital video pixel clock output
75	TEST	I, PD	Manufacture test mode, connect to GND
76	GPIO0	I/O, PD	GPIO 0
77	GPIO1	I/O, PD	GPIO 1
78	MCU_D0	I/O , PD	MCU NOR flash interface data bus bit 0

PIN NUMBER			
79	MCU_D1	I/O , PD	MCU NOR flash interface data bus bit 1
80	UART_TXD	O	High speed UART data output
	GPIO14	O	GPIO 14 , only can be used as output mode
	SPI_MOD	I, PD	Hardware strap pin : SPI_MOD
81	UART_RXD	I, PD	High speed UART data input
	GPIO15	I/O , PD	GPIO 15
82	MCU_D2	I/O , PD	MCU NOR flash interface data bus bit 2
83	MCU_D3	I/O , PD	MCU NOR flash interface data bus bit 3
84	GPIO2	I/O, PD	GPIO 2
85	GPIO3	I/O, PD	GPIO 3
	TV_CLK_O	O	TV 27MHZ CLK output
86	MCU_D4	I/O , PD	MCU NOR flash interface data bus bit 4
87	MCU_D5	I/O , PD	MCU NOR flash interface data bus bit 5
88	GPIO10	I/O , PD	GPIO 10
89	SPI_SS	I/O, PU	SPI master interface slave select output
	GPIO10	I/O, PU	GPIO 10
90	SPI_SCK	I/O, PD	SPI master interface serial clock output
	GPIO11	I/O, PD	GPIO 11
91	SPI_MOSI	I/O, PD	SPI master interface master output
	GPIO12	I/O, PD	GPIO 12
92	SPI_MISO	I/O, PD	SPI master interface slave input
	GPIO13	I/O, PD	GPIO 13
93	MCU_D6	I/O, PD	MCU NOR flash interface data bus bit 6
94	MCU_D7	I/O, PD	MCU NOR flash interface data bus bit 7
95	CS_ENB	O	Sensor enable pin, Output
	SIF_EDG	I, PD	Hardware strap pin: SIF_EDG
96	MCU_OEN	O	MCU NOR flash interface external memory output enable , “0” valid
97	MCU_PCEN	O	MCU NOR flash interface code memory chip select , “0” valid
98	VDD	P	Digital core Power 1.2V
99	VSS	P	Digital IO/core ground
100	VDD_IO	P	Digital IO Power 3.3V

4.2 VC0706PTNA Pin Assignments

PIN NUMBER VC0706PTNA	NAME	TYPE	DESCRIPTION
1	NC		No connect
2	NC		No connect
3	NC		No connect
4	CS_SDA	I/O, OD , S	Sensor I2C bus SDA pin
5	GPIO13	I/O, PD	GPIO 13
6	CS_SCK	I/O, OD , S	Sensor I2C bus SCK pin
7	GPIO12	I/O , PD	GPIO 12
8	CS_HSYNC	I, PD	Sensor Horizontal sync input
9	MCU_WEN	O	MCU NOR flash interface write enable signal "0" indicate write operation; "1" indicate read operation
10	CS_VSYNC	I, PD	Sensor vertical sync input
11	MCU_A15	O	MCU NOR flash interface address bit 15
12	MCU_A14	O	MCU NOR flash interface address bit 14
13	VDD	P	Digital Core Power, 1.2v
14	CS_PCLK	I, PD	Sensor pixel clock input
15	VSS	P	Digital IO/Core ground
16	CS_CLK	O	Sensor CLK output
17	VDD_IO	P	Digital IO power, 3.3v
18	GPIO9	I/O , PD	GPIO 9
	OSD_RDY	O	Ready to accept new OSD data from host through SPI interface
19	CS_D0	I, PD	Sensor data input bit 0
	CS_PCLK	I, PD	Sensor pixel clock input
20	MCU_DCEN	O	MCU NOR flash interface data memory chip select , "0" valid
21	CS_D1	I, PD	Sensor data input bit 1
22	CS_D2	I, PD	Sensor data input bit 2
23	MCU_A13	O	MCU NOR flash interface address bit 13
24	MCU_A12	O	MCU NOR flash interface address bit 12
25	VDD_IO	P	Digital IO power, 3.3v

PIN NUMBER			
26	VSS	P	Digital IO/core ground
27	VDD	P	Digital core power, 1.2v
28	CS_D3	I, PD	Sensor data input bit 3
29	CS_D4	I, PD	Sensor data input bit 4
30	MCU_A11	O	MCU NOR flash interface address bit 11
31	MCU_A10	O	MCU NOR flash interface address bit 10
32	CS_D5	I, PD	Sensor data input bit 5
33	CS_D6	I, PD	Sensor data input bit 6
34	MCU_A9	O	MCU NOR flash interface address bit 9
35	NC		Not connect
36	NC		Not connect
37	GPIO8	I/O, PD	GPIO 8
	OSD_STOP	I, PD	Host asserted signal to stop OSD DMA
38	MCU_A8	O	MCU NOR flash interface address bit 8
39	CS_D7	I, PD	Sensor data input bit 7
40	CS_D8	I, PD	Sensor data input bit 8
41	CS_D9	I, PD	Sensor data input bit 9
42	VDD_IO	P	Digital IO power , 3.3v
43	MCU_A7	O	MCU NOR flash interface address bit 7
44	VSS	P	Digital IO/Core ground
45	MCU_A6	O	MCU NOR flash interface address bit 6
46	VDD	P	Digital core power , 1.2v
47	CS_PWD	O	CMOS Sensor Power Down Control
	GPIO5	O	GPIO 5 , only can be used as output mode
	TV_HSYNC_O	O	TV encoder HSYNC output
48	CS_RSTB	O	Sensor Reset Output
	TV_MOD	I, PD	Hardware strap pin : TV_MOD
49	MCU_A5	O	MCU NOR flash interface address bit 5
50	MCU_A4	O	MCU NOR flash interface address bit 4
51	GPIO7	I/O , PD	GPIO 7
52	RSTN	I , PU	Power on reset
53	GPIO4	I/O, PD	GPIO 4
	TV_VSYNC_O	O	TV Vertical SYNC Output

PIN NUMBER			
	TV_CSYNC_O	O	TV Composite SYNC Output
54	GPIO11	I/O , PD	GPIO 11
55	MCU_A3	O	MCU NOR flash interface address bit 3
56	MCU_A2	O	MCU NOR flash interface address bit 2
57	MCU_A1	O	MCU NOR flash interface address bit 1
	OCODE_MOD	I , PD	Hardware strap pin : OCODE_MOD
58	MCU_A0	O	MCU NOR flash interface address bit 0
	OROM_MOD	I , PD	Hardware strap pin : OROM_MOD
59	VDD_IO	P	Digital IO Power 3.3V
60	VSS	P	Digital IO/core ground
61	VDD	P	Digital core power , 1.2v
62	VFB	A	Test signal , not connect
63	VOUT	A	Test signal , not connect
64	VSSA	P	Analog ground
65	VSSA	P	Analog ground
66	VSSA	P	Analog ground
67	MONA	A	Test signal , not connect
68	VDDA	P	Analog power supply ,3.3V
69	VDDA	P	Analog power supply ,3.3v
70	VDDA	P	Analog power supply ,3.3v
71	ONKEYZ	A	Test pin, need connect to VDDA
72	NC		No connect
73	VLX	A	Test signal , not connect
74	VLX	A	Test signal , not connect
75	VSSA	P	Analog ground
76	VSSA	P	Analog ground
77	ONKEYZ	A	Test pin, need connect to VDDA
78	DAC_REXT	A	DAC external resistor pin
79	DAC_COMP	A	DAC Compensation pin
80	DAC_CVBS	A, O	CVBS channel signal analog output
81	VSSA_SUB	P	DAC pad ground
82	VSSA_DAC	P	DAC analog ground
83	VDDA_DAC	P	DAC analog power ,3.3v
84	VDDA_WELL	P	DAC pad Power ,3.3V

PIN NUMBER			
85	VSS_PLL	P	Digital core ground for DAC/PLL
86	VDD_PLL	P	Digital core power for DAC/PLL ,1.2v
87	VSSA_PLL	P	PLL Analog ground
88	VDDA_PLL	P	PLL Analog power ,3.3V
89	TV_D7	O	CCIR656 digital video output bit 7
90	VDD	P	Digital core power ,1.2v
91	TV_D6	O	CCIR656 digital video output bit 6
92	VSS	P	Digital IO/core ground
93	TV_D5	O	CCIR656 digital video output bit 5
94	TV_D4	O	CCIR656 digital video output bit 4
95	GPIO6	I/O , PD	GPIO 6
	TV_ODD_O	O	TV encoder ODD signal output , “Low” indicate even field , “High” indicate odd field
96	TV_D3	O	CCIR656 digital video output bit 3
97	TV_D2	O	CCIR656 digital video output bit 2
98	GPIO5	O	GPIO 5 , only can be used as output mode
	TV_HSYNC_O	O	TV encoder HSYNC output
	BOOT_MOD	I, PD	Hardware strap pin : BOOT_MOD
99	TV_D1	O	CCIR656 digital video output bit 1
100	TV_D0	O	CCIR656 digital video output bit 0
101	TV_VSYNC	O	TV vsync output
102	TV_HSYNC	O	TV hsync output
103	VDD	P	Digital core power , 1.2v
104	CLK_IN	I	Crystal input
105	CLK_OUT	O	Crystal output (loopback)
106	VSS	P	Digital IO/CORE ground
107	VDD_IO	P	Digital IO Power ,3.3v
108	TV_PCLK	O	Digital video pixel clock output
109	TEST	I, PD	Manufacture test mode, connect to GND
110	NC		Not connect
111	NC		Not connect
112	NC		Not connect
113	GPIO0	I/O, PD	GPIO 0
114	VDD_IO	P	Digital IO power, 3.3v

PIN NUMBER			
115	GPIO1	I/O, PD	GPIO 1
116	MCU_D0	I/O , PD	MCU NOR flash interface data bus bit 0
117	VSS	P	Digital IO/core ground
118	MCU_D1	I/O , PD	MCU NOR flash interface data bus bit 1
119	VDD	P	Digital core power, 1.2v
120	UART_TXD	O	High speed UART data output
	GPIO14	O	GPIO 14 , only can be used as output mode
	SPI_MOD	I, PD	Hardware strap pin : SPI_MOD
121	UART_RXD	I, PD	High speed UART data input
	GPIO15	I/O , PD	GPIO 15
122	MCU_D2	I/O , PD	MCU NOR flash interface data bus bit 2
123	MCU_D3	I/O , PD	MCU NOR flash interface data bus bit 3
124	GPIO2	I/O, PD	GPIO 2
125	GPIO3	I/O, PD	GPIO 3
	TV_CLK_O	O	TV 27MHZ CLK output
126	MCU_D4	I/O , PD	MCU NOR flash interface data bus bit 4
127	MCU_D5	I/O , PD	MCU NOR flash interface data bus bit 5
128	GPIO10	I/O , PD	GPIO 10
129	SPI_SS	I/O, PU	SPI master interface slave select output
	GPIO10	I/O, PU	GPIO 10
130	VDD	P	Digital core power , 1.2v
131	SPI_SCK	I/O, PD	SPI master interface serial clock output
	GPIO11	I/O, PD	GPIO 11
132	VSS	P	Digital IO/core ground
133	SPI_MOSI	I/O, PD	SPI master interface master output
	GPIO12	I/O, PD	GPIO 12
134	VDD_IO	P	Digital IO power , 3.3v
135	SPI_MISO	I/O, PD	SPI master interface slave input
	GPIO13	I/O, PD	GPIO 13
136	MCU_D6	I/O, PD	MCU NOR flash interface data bus bit 6
137	MCU_D7	I/O, PD	MCU NOR flash interface data bus bit 7
138	CS_ENB	O	Sensor enable pin, Output
	SIF_EDG	I, PD	Hardware strap pin: SIF_EDG

PIN NUMBER			
139	MCU_OEN	O	MCU NOR flash interface external memory output enable , “0” valid
140	MCU_PCEN	O	MCU NOR flash interface code memory chip select , “0” valid
141	VDD	P	Digital core Power 1.2V
142	VSS	P	Digital IO/core ground
143	LDOM	I	Test pin, connect to GND
144	VDD_IO	P	Digital IO Power 3.3V

Note: I/O – Bidirectional Input/Output
I – Input
O – Output
P – Power
G – Ground
A – Analog
PD – Internal Pull Up
PU – Internal Pull Down
OD – Open Drain
S – Schmitt Trigger
A – Analog Links (to a resistor, capacitor etc.)

4.3 Hardware Strap Pin Descriptions

VC0706 has hardware strap pins. Those pins are multiplex usage pins. When the VC0706 had been reset, the pull-up or pull-down status of these pins will set the configuration of VC0706.

The table below lists the hardware strap pins and their functions:

In the table, 0 means pull-down, 1 means pull-up, the on-chip pull-down resisters will select the default setting if no external resistors used to pull-up the hardware strap pins.

SIGNAL NAME	DESCRIPTION
TV_MOD	Used for the selection of TV 525 lines or 625 lines output mode 0 (default): 525 lines, NTSC TV system 1: 625 lines, PAL TV system
SIF_EDGE	Used for the selection of the clock edge for sensor-interface sampling sensor’s input data 0(default): use default setting for sampling 1: use reverse edge for sampling
BOOT_MOD	Used for the selection of host boot enable or disable

	0(default): Host boot disable 1 : Host boot enable
SPI_MOD	Used for the selection of SPI interface work in master mode or slave mode 0(default) : SPI interface work in master mode 1 : SPI interface work in slave mode
OROM_MOD	Used for the selection of boot from internal ROM or external ROM 0(default) : MCU boot from internal ROM 1 : MCU boot from external ROM
OCODE_MOD	Used for the selection of external code ROM working under normal mode or encryption mode 0(default) : Normal mode 1 : Encryption mode

4.4 VC0706PREA (100-Pin LQFP) Pin Layout Diagram

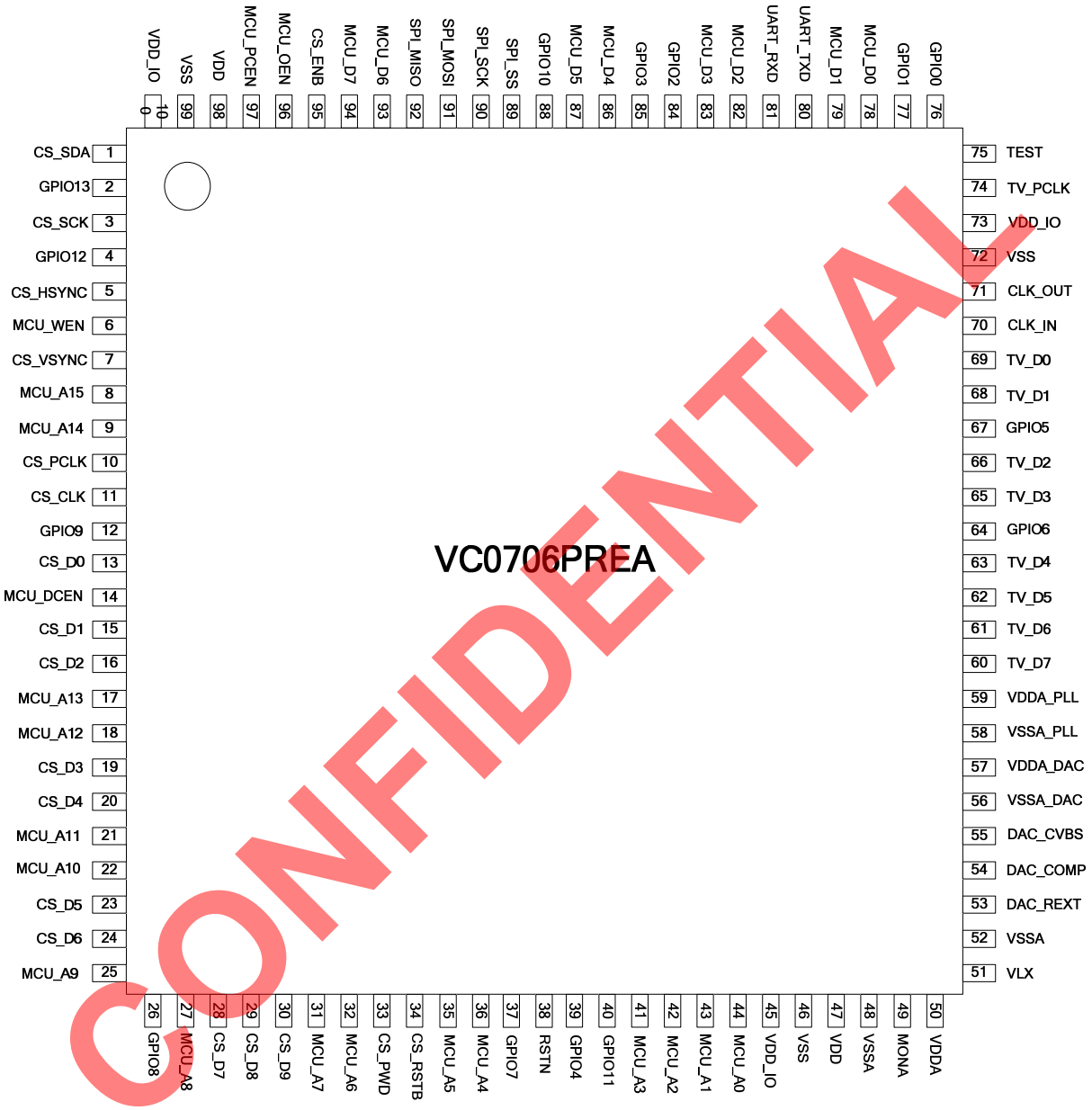


Figure 2: VC0706PREA Pin Layout Diagram

4.5 VC0706PTNA (144-Pin LQFP) Pin Layout Diagram

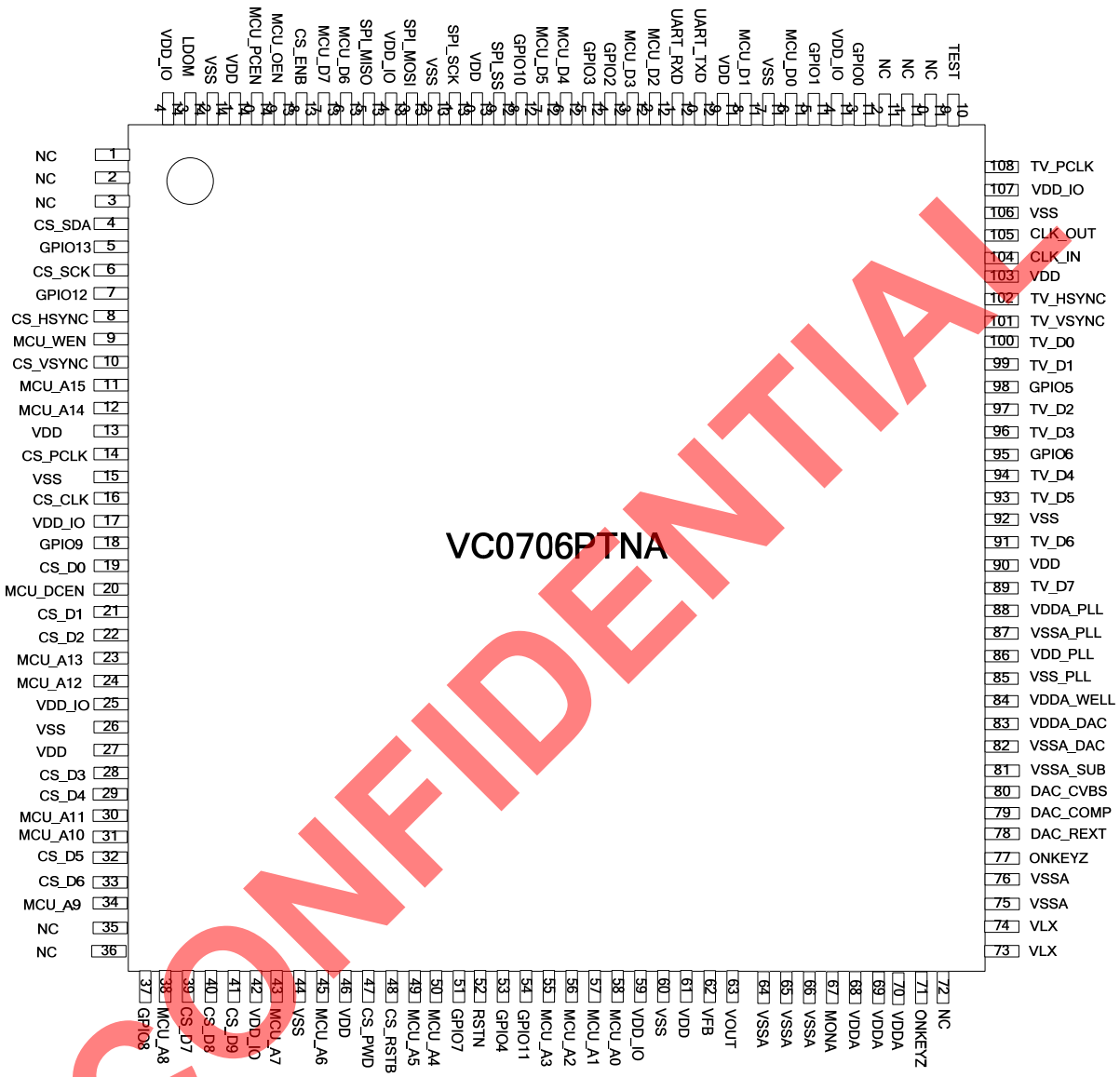


Figure 3: VC0706PTNA Pin Layout Diagram

5. ELECTRICAL CHARACTERISTICS

5.1. Recommended Operating Conditions

The recommended operating conditions are the recommended values to assure normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) described below are assured.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD_IO	I/O Digital Voltage (3.3V)	2.97	3.3	3.63	V
VDD_CORE	Core Digital Voltage	1.08	1.2	1.32	V
VDDA_DAC	Video DAC Voltage	2.97	3.3	3.63	V
VDDA_PLL	PLL Voltage	2.97	3.3	3.63	V
VDDA	Analog Voltage	2.97	3.3	3.63	V
T_O	Operating Temperature	-40	-	+85	ºC
T_S	Storage Temperature	-40	-	+125	ºC

5.2. Digital I/O Electrical Characteristics

For 3.3V I/O Application

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input low voltage	V_{IL}	-0.3	-	0.8	V
Input high voltage	V_{IH}	2.0	-	VDD_IO+0.3	V
Threshold point	V_T	1.30	1.41	1.53	V
Schmitt trig low to high threshold point	V_{T+}	1.54	1.65	1.74	V
Schmitt trig high to low threshold point	V_{T-}	0.95	1.02	1.09	V
Input leakage current	I_L	-	-	±1	μA
Input pull-up resistor	R_{PU}	62	77	112	kΩ

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input pull-down resistor	R_{PD}	58	81	156	kΩ
Output low voltage	V_{OL}	-	-	0.4	V
Output high voltage	V_{OH}	2.4	-	-	V
Low level output current @ V_{OL}=0.4V	I_{OL}	4.2	6.6	8.1	mA
High level output current @ V_{OH}=2.4V	I_{OH}	4.7	9.6	14.9	mA

5.3. Video DAC Electrical Characteristics

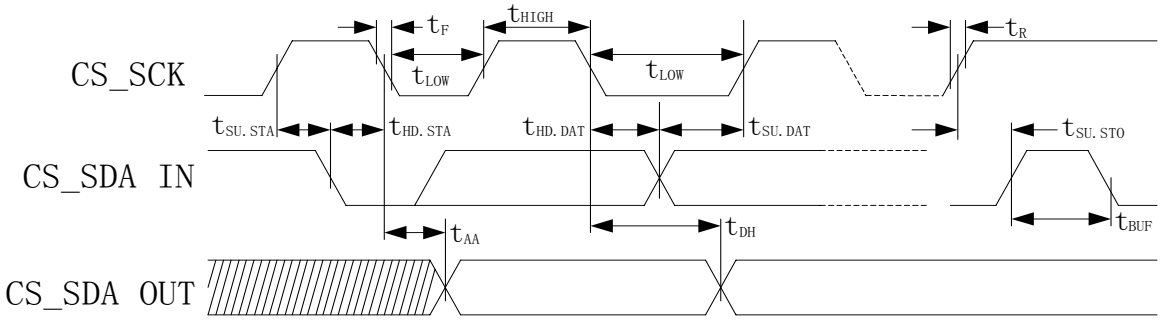
(VDDA_DAC = 3.3V , RL=37.5ohm , CL=10pF , VREFIN=1.20V; TEMP = 25°c)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Max per-channel output current	Ifs	-	34.8	-	mA
Max output voltage	Vfs	-	1.304	-	V
DAC resolution	-	-	10	-	bits
Integral non-linearity error	ERRinl	-	±1	±1.5	LSB
Differential non-linearity error	ERRdnl	-	±0.5	±1	LSB

5.4. AC Electrical Characteristics

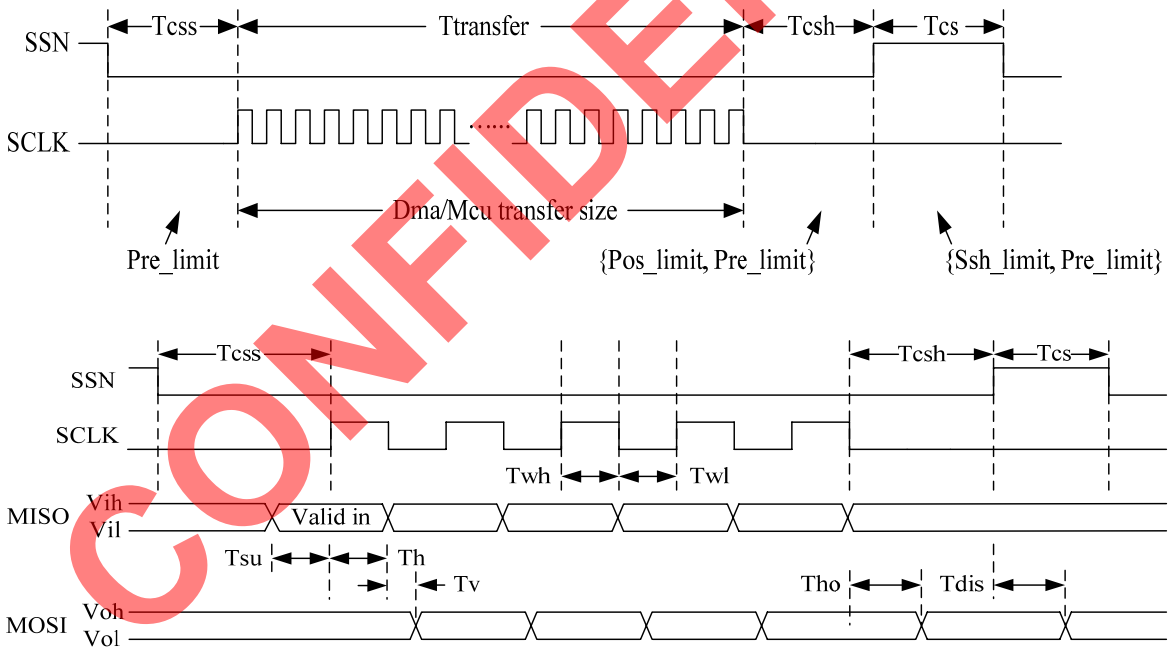
This section describes the AC characteristics of VC0706, including output delays, input setup, hold times, and all the interface timing.

5.4.1. I²C Interface Timing Specification



PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS_SCK clock frequency	f_{SCK}			400	kHz
Bus free time between a STOP and a START	t_{BUF}	4.7		-	us
Hold time for a START	$t_{HD;STA}$	4.0		-	us
Low period of CS_SCK	t_{LOW}	4.7		-	us
High period of CS_SCK	t_{HIGH}	4.0		-	us
Setup time for START	$t_{SU;STA}$	4.7		-	us
Data hold time	$t_{HD;DAT}$	0		-	us
Data setup time	$t_{SU;DAT}$	200		-	ns
Rise time of CS_SDA and CS_SCK	t_R	-		1	us
Fall time of CS_SDA and CS_SCK	t_F	-		300	ns
CS_SCK low to data out valid	t_{AA}	0.625			us
Data out hold time	t_{DH}	0.625			us
Setup time for STOP	$t_{SU;STO}$	4.7		-	us

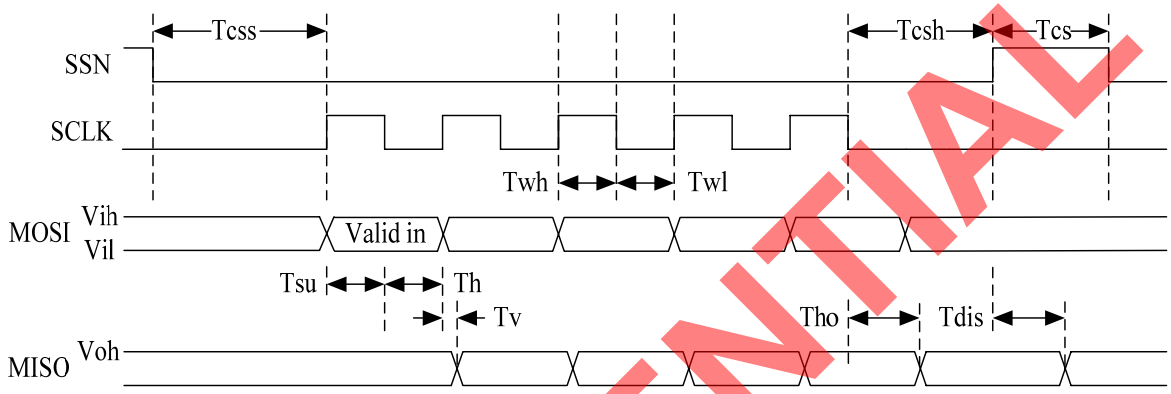
5.4.2. SPI Master Interface Timing Specification



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fsclk	SCLK clock frequency	0	-	18	MHz
Twh	SCLK high time	25	-	-	ns
Twl	SCLK low time	25	-	-	ns
Tcs	SSN high time	56	-	-	ns
Tcss	SSN setup time	56	-	-	ns
Tcsh	SSN hold time	56	-	-	ns

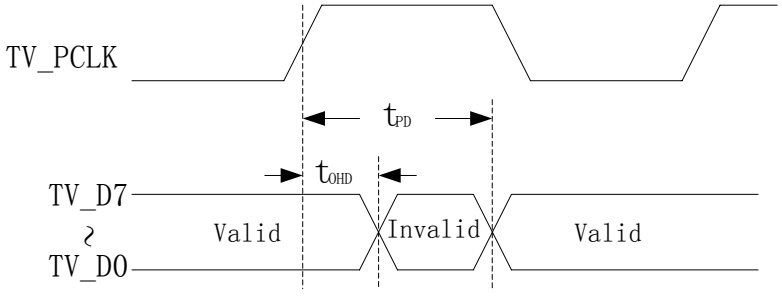
Tsu	Data in setup time	3	-	-	ns
Th	Data in hold time	3	-	-	ns
Tv	Output valid	-	-	3	ns
Tho	Output hold time	0	-	-	ns
Tdis	Output disable time	-	-	56	ns

5.4.3. SPI Slave Interface Timing Specification



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Fsclk	SCLK clock frequency	0	-	17	MHz
Twh	SCLK high time	28	-	-	ns
Twl	SCLK low time	28	-	-	ns
Tcs	SSN high time	56	-	-	ns
Tcss	SSN setup time	112	-	-	ns
Tcsh	SSN hold time	56	-	-	ns
Tsu	Data in setup time	3	-	-	ns
Th	Data in hold time	3	-	-	ns
Tv	Output valid	-	-	10	ns
Tho	Output hold time	32	-	-	ns
Tdis	Output disable time	-	-	56	ns

5.4.4. CCIR656 Timing Characteristics



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
C_L	output load capacitance		15	---	40	pF
t_{OHD}	output hold time	C_L = 15pF	1.3	---	---	ns
t_{PD}	propagation delay	C_L = 25pF	---	---	7.9	ns

	Field Line Number		Active Line Number	
	525	625	525	625
Field 1 (F = 0)	4 ~ 265	1 ~312	20 ~ 263	23 ~ 310
Field 2 (F = 1)	266 ~ 3	313 ~ 625	283 ~ 525	336 ~ 623

Note: 1. When frame has 486 active lines for 525 system, line 263 is black.

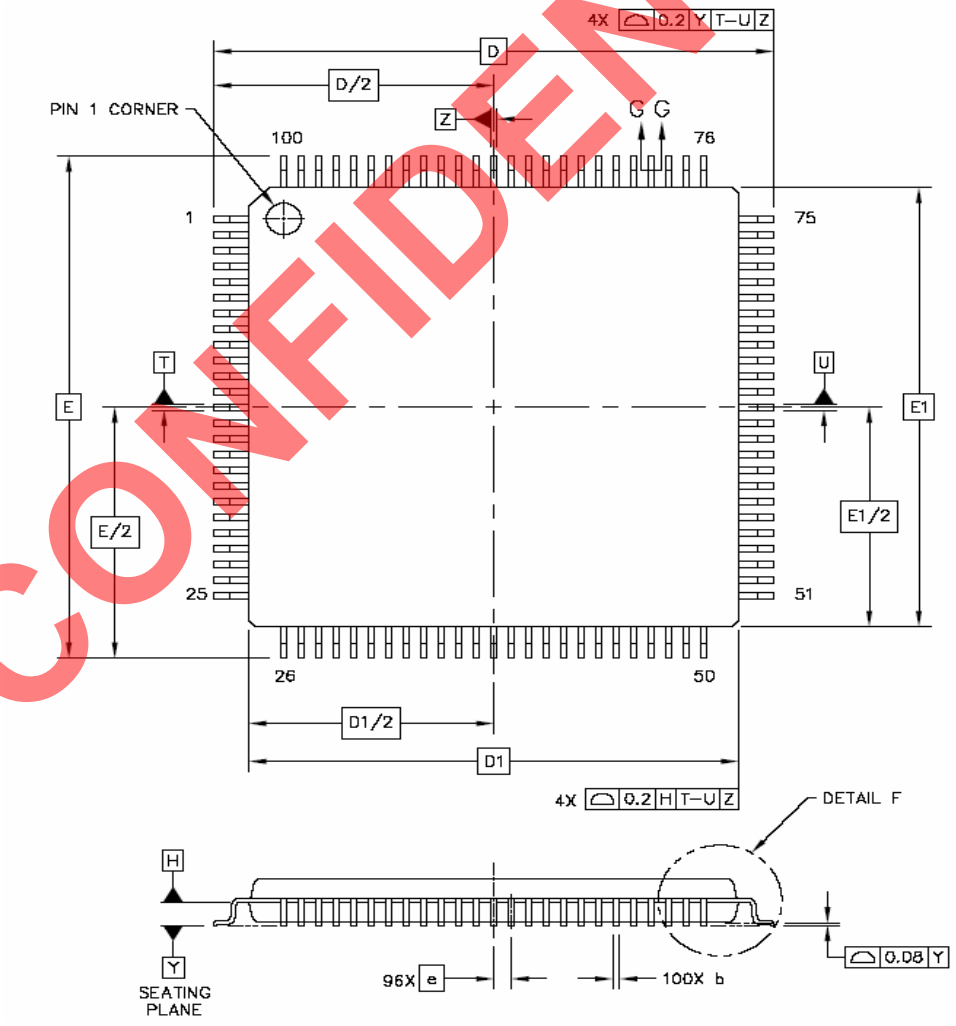
2. When frame has 480 active lines for 525 system, field 1 line 20, 21, 22, 263 are and field 2 line 283, 284, 285 are black.

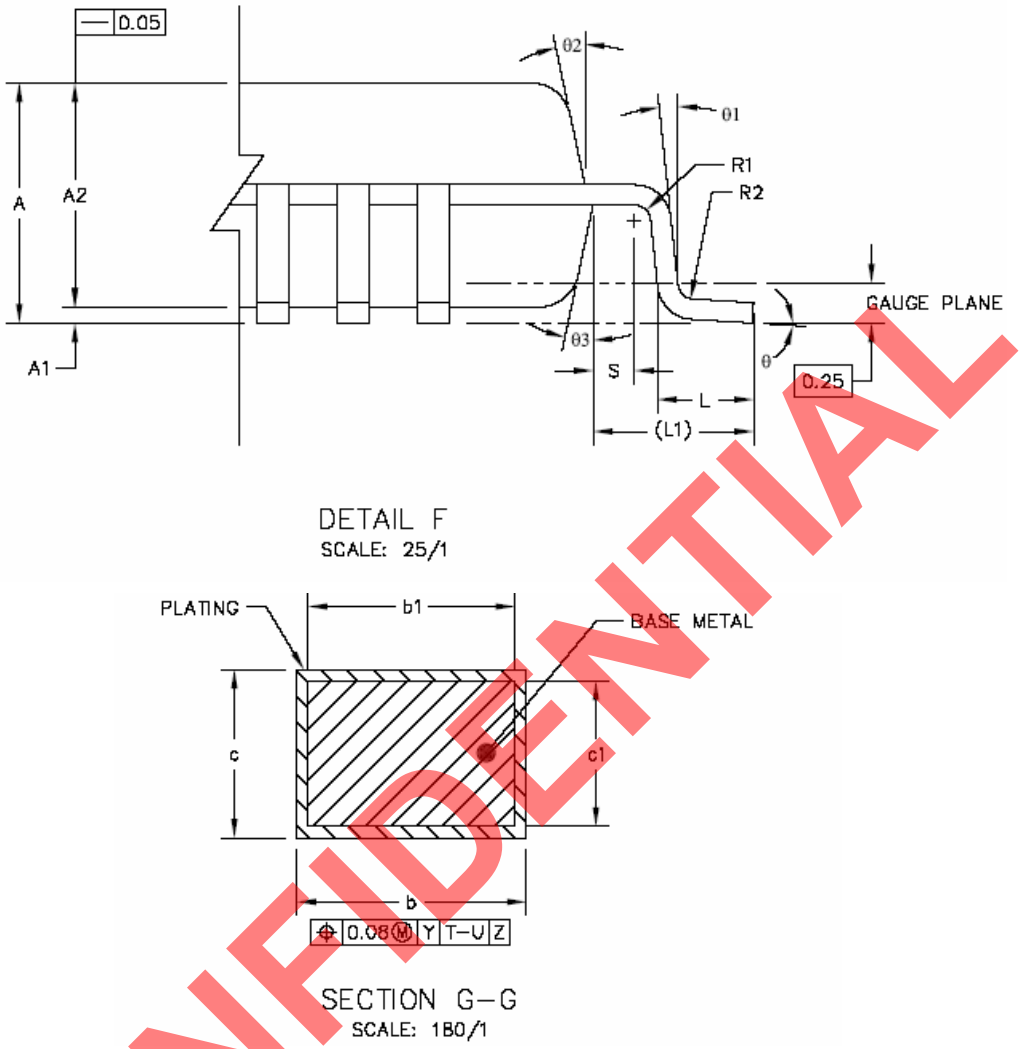
6. PACKAGE INFORMATION

6.1. Chip Marking Information

MARKING INFORMATION	LEAD-FREE PACKAGE
	Vimicro VC0706PREA Tracking No.
	Vimicro VC0706PTNA Tracking No.

6.2. VC0706PREA Package Specification (14mm x 14mm)





PACKAGE	LQFP 100L 14*14* 0.9 – 0.5		
DIM	MIN.	NOM.	MAX.
A	---	---	1.6
A1	0.05	---	0.15
A2	1.35	1.4	1.45
b	0.17	0.2	0.27
b1	0.17		0.23
c	0.09		0.2
c1	0.09		0.16
D	16 BSC		
D1	14 BSC		
e	0.5 BSC		
E	16 BSC		
E1	14 BSC		
L	0.45	0.6	0.75
L1	1 REF		
R1	0.08		---
R2	0.08		0.2

S	0.2		---
θ	0	3.5	7
θ1	0		---
θ2	11	12	13
θ3	11	12	13

NOTES:

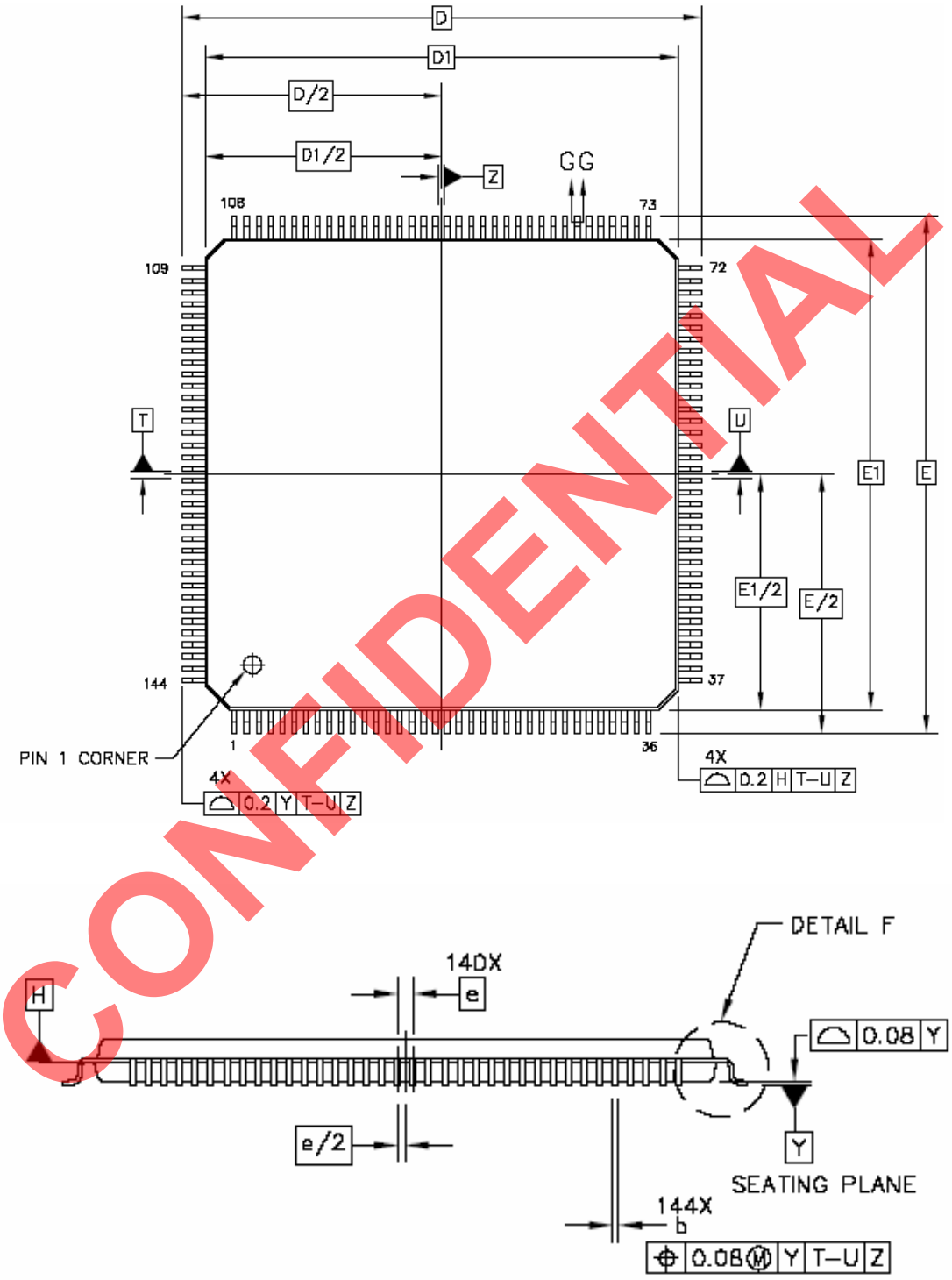
⌘ DIMENSIONS ARE IN MILLIMETERS .

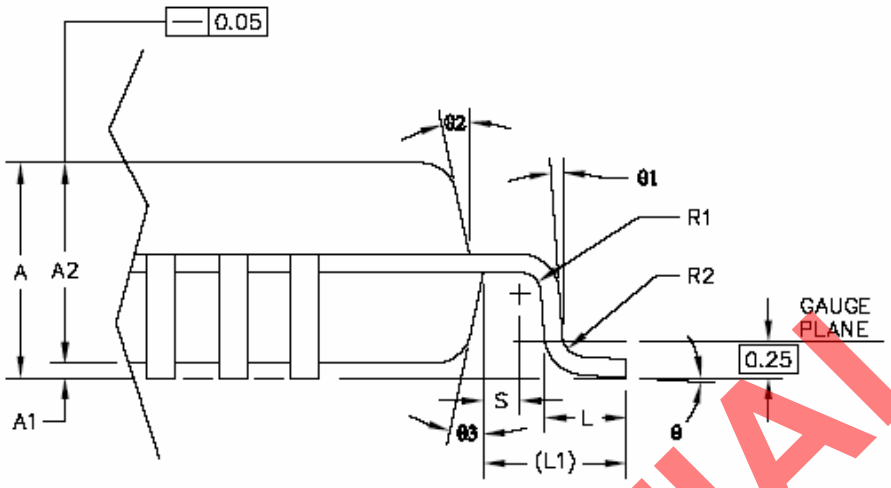
⌘ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH .

⌘ INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M --- 1994.

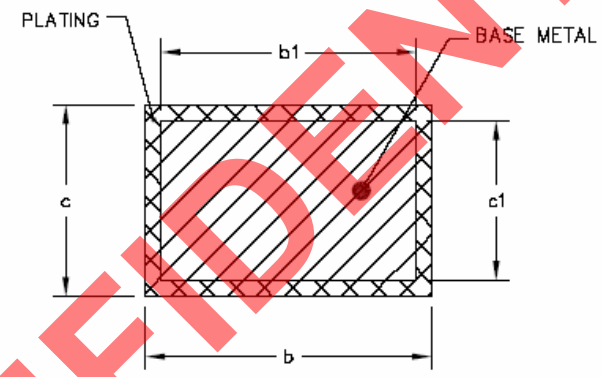
⌘ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm . DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT . MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm AND 0.5mm PITCH PACKAGES.

6.3. VC0706PTNA Package Specification (20mm x 20mm)





DETAIL F



SECTION G–G

PACKAGE	LQFP 100L 14*14* 0.9 – 0.5		
DIM	MIN.	NOM.	MAX.
A	---	---	1.6
A1	0.05	---	0.15
A2	1.35	1.4	1.45
b	0.17	0.22	0.27
b1	0.17	0.2	0.23
c	0.09		0.2
c1	0.09		0.16
D	22 BSC		
D1	20 BSC		
e	0.5 BSC		
E	22 BSC		
E1	20 BSC		
L	0.5	0.6	0.75
L1	1 REF		

R1	0.08		---
R2	0.08		0.2
S	0.2		---
θ	0	3.5	7
θ1	0		---
θ2	11	12	13
θ3	11	12	13

NOTES:

⌘ DIMENSIONS ARE IN MILLIMETERS .

⌘ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH .

⌘ INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M --- 1994.

⌘ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm . DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT . MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.5mm PITCH PACKAGES .

7. CONTACT INFORMATION

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8. REVISION HISTORY

Version No.	Remarks	Release Date
0.1	Initial draft released for review.	2007-8-15
0.9	Preliminary release.	2007-8-23
1.0	Merge VC0706PTNA and update block diagram, product description	2007-9-28